IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 15472US02

In re Application of:	)	
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Pai	)	**Electronically Filed**
	)	
Serial No.: 10/816,320	)	**Date: March 10, 2010**
	)	
Filing Date: 4/1/2004	)	
	)	
Examiner: Holder	)	
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Confirmation No.: 9138	)	
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Art Unit No. 2621	)	
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PRE-APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This amendment is filed in response to the Office Action mailed 11/10/09.

REMARKS

Claims 1, 2, 4-9, 11-15, and 17-20 are presently pending. Claims 3, 10, and 16 are cancelled without prejudice. Appellant appeals certain rejections and requests pre-appeal review.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious from Wise, Abelard, and Kato. Claim 1 recites, among other limitations, "the parameters comprising a picture type indicator for indicating a type of a picture; and logic for determining whether the parameters received by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input".

Examiner has indicated that Wise teaches:

Logic for determining whether the parameters received by the input are valid [Fig. 23, 131, 127, P0505, 0510, 2073, 2079, 2236];

Wise, Figure 23 shows "a Spatial Decoder DRAM interface" [0108]. Wise Figure 127 is a buffer manager [2073]. Wise, Figure 131 describes a DRAM interface [2234]. P505 discusses an "address generator". P510 discusses control interfaces between the address generator. While P2073 poses the the question "is it a valid address"?

While Wise discusses progressive and interlaced pictures, clearly the alleged logic [Fig. 23, 131, 127, P0505, 0510, 2073, 2079, 2236] does not teach to determine the validity of anything *based on whether the picture is progressive or interlaced.*

Wise, Figures 23, 127, 131 are shown below:

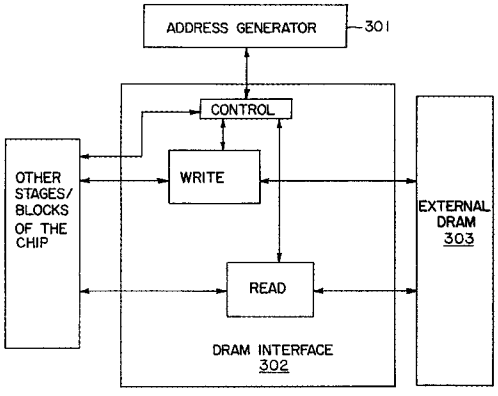

FIG.23

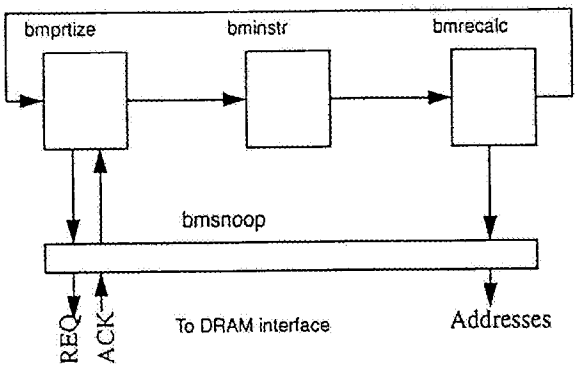

FIG. 127

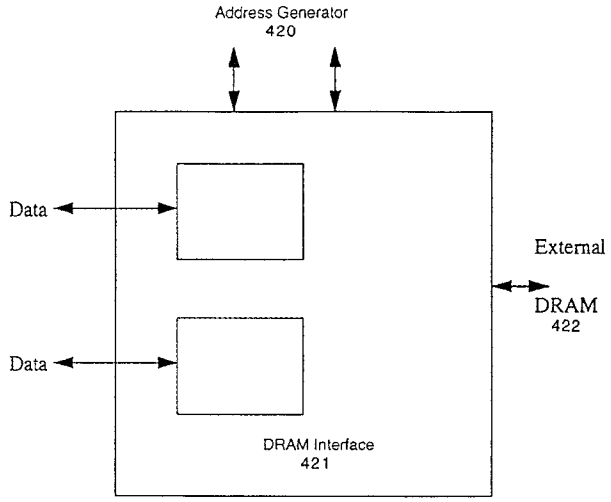

FIG. 131

It can be seen that whether the picture is progressive or interlaced is not even an input to the "logic" in Wise.

The Office Action concedes that Wise does not teach determining whether the input are valid based on the picture type indicator and the number of motion vectors. However, the Office Action finds picture type indicator in Abelard, and number of motion vectors in Kato.

Appellant respectfully submits that from the DRAM interfaces in Wise, and the mere existance of progressive and interlaced pictures, picture type indicators, and counting the number of motion vectors, "logic for determining whether the parameters received by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input" would not be obvious.

To begin with, as can be seen in the foregoing figures, it is unclear how the logic in Wise, which appears to determine the validity of an address, could even be adapted to receive information such as picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input.

Moreover, if somehow, Wise was so adapted, none of the references provide any criteria, rules, algorithms, truth tables, or the like, correlating validity of something based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input.

Accordingly, Appellant requests reversal of the rejections to claims 1, 8, and 13.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Wise, Abeland, and Kato in view of Kim. Claim 5 recites, among other limitations, "wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Examiner has indicated that Wise, Kato, and Abelard, modified by Kim teaches the foregoing, at [Kim – Abstract; col. 1 lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6, Lines 8-12; col. 5, line 57 – col. 6 line 20].

Although in Kim, Abstract, the "motion vector decoder" includes a number of things, e.g., "a parameter delay block", "a motion vector residual block", "motion vector code table", etc., Kim abstract does not teach anything that "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Moreover, Kim, Col. 6, Lines 8-12 recites that:

> The vlc[10:0], shown in FIG. 2(e), is a MV value variable length coded by the encoder and is received by the MV residual block 11 and the MV code table block. Since maximum of 11 data bits may be produced through the VLC, the vlc[10:0] has a length of 11 bits and is the most significant bit (msb). The msb value may or may not be sent by the encoder and if sent, one or all eight values may be sent.

(Emphasis Added). It is noted that Kim does not tech that "vlc[10:0]" "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector

registers". Moreover, it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44. Thus vlc[10:0] does not "comprise[s] one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Examiner has also indicated that "Kim discloses 8 bit number in the residual value. [col. 5 line 57 –col. 6 line 20]". Office Action at 2. Assignee has not disputed that Kim discloses "one or more bits", rather, Assignee traverses the finding that Kim discloses one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector". The argument in the above paragraph (it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44…) would apply the same to 8 bits.

Accordingly, Appellant requests reversal of the rejection to claim 5.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: March 10, 2010

Respectfully submitted,

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